Invention relates to computing technology and can be used in specialized computer systems, digital signal processing systems and neural networks to increase a range of variation of input data values when calculating a scalar product with pre-known multipliers (constants). Device for calculating a scalar product comprises an input for a maximum order of macro-partial products, three write inputs, four control inputs, two clock inputs, an input for an input data order, an input for an input data mantissa, an address input, a data input, a memory operating mode selection input, a memory select input, a reset input, a maximum order register for macro-partial products, an input data loading unit comprising k order registers, where k is a number of product pairs, and k mantissa registers, a maximum order determination unit comprising an order register, an order switch, an AND logic element, a subtractor, a higher order register, a maximum order register, an address register, a data register, a NOT-OR logic element, k nodes for order alignment and address bit formation, wherein each s-th node, where s=1,…, k, comprises an order register, a mantissa register, a subtractor, a first switch, a comparison circuit and a second switch, an OR logic element, an order adder, an address switch, a memory, a macro-partial product register, a macro-partial product adder-subtractor, a scalar product order register, a scalar product mantissa register, a scalar product order output, and a scalar product mantissa output. Technical result: increasing the range of variation of input data values when calculating the scalar product with pre-known multipliers by using a floating-point format.