Device for diagnosing the braking circuits of frequency-controlled asynchronous electric drives, comprising a switch, six comparators, two OR gates, three pulse counting devices, a register, two pulse generators, an display unit, two pulse generators, six AND gates, six NOT gates, a current sensor, a voltage sensor, a temperature sensor, a minimum current value unit, a maximum current value unit, minimum voltage unit, maximum voltage unit, minimum temperature unit, maximum temperature unit, seven flip-flops, three XOR gates, braking start unit, zero-reset unit, decoder, sample logic-time function unit, and a digital comparator. The output of the current sensor is connected to the second input of the first comparator and to the first input of the second comparator, whose second input is connected to the output of the maximum current value unit. The output of the minimum current value unit is connected to the first input of the first comparator, whose output is connected to the first input of the first NOT gate, whose output is connected to the first input of the first flip-flop, whose output is connected to the first input of the first AND gate. The output of the second comparator is connected to the first input of the second NOT gate, whose output is connected to the first input of the second flip-flop, whose output is connected to the second input of the first AND element. The output of the voltage sensor is connected to the second input of the third comparator and to the first input of the fourth comparator, whose second input is connected to the output of the maximum voltage value unit. The output of the minimum voltage value unit is connected to the first input of the third comparator, whose output is connected to the first input of the third NOT element, whose output is connected to the first input of the third flip-flop, whose output is connected to the first input of the second AND element. The output of the fourth comparator is connected to the first input of the fourth NOT element, whose output is connected to the first input of the fourth flip-flop, whose output is connected to the second input of the second AND element. The output of the temperature sensor is connected to the second input of the fifth comparator and to the first input of the sixth comparator, whose second input is connected to the output of the maximum temperature unit, and the output of the minimum temperature unit is connected to the first input of the fifth comparator, whose output is connected to the first input of the fifth NOT gate, whose output is connected to the first input of the fifth flip-flop, whose output is connected to the first input of the third AND element. The output of the sixth comparator is connected to the first input of the sixth NOT element, whose output is connected to the first input of the sixth flip-flop, whose output is connected to the second input of the third AND element. The outputs of the first, second, and third AND gates are connected, respectively, to the first inputs of the first, second, and third XOR gates. The output of the fourth AND gate is connected to the first input of the first pulse counter and to the input of the first pulse generator; the output of the first pulse generator is connected to the first input of the fourth AND gate. The output of the braking start unit is connected to the second input of the fourth AND gate and is connected to the first input of the first OR gate, the second input of which is connected to the output of the zero-reset unit, and whose output is connected to the second inputs of the first pulse counter, the first, second, third, fourth, fifth, and sixth flip-flops, the first, second, third, fourth, fifth, and sixth NOT elements, as well as to the first input of the second OR element and to the second input of the register. The output digital bus of the first pulse counter is connected to the input digital bus of the decoder, whose output digital bus is connected to the input digital bus of the reference logic-time function unit and to the second input digital bus of the register. The decoder's output is connected to the third input of the first OR element and to the synchronization input of the display unit. The first, second, and third outputs of the sample logic-time function unit are connected, respectively, to the second inputs of the first, second, and third XOR elements, whose outputs are connected to the first, second, and third inputs of the switch, respectively. The output of the first pulse generator is connected to the first input of the seventh flip-flop, whose output is connected to the first input of the fifth AND gate; the second input of the fifth AND gate is connected to the output of the second pulse generator, and its output is connected to the first input of the second pulse counting device and to the second input of the sixth AND gate. The first and second outputs of the second pulse counting device are connected, respectively, to the fourth and fifth inputs of the switch, whose

output is connected to the first input of the sixth AND gate. The third output of the second pulse counting device is connected to the input of the digital comparator and to the second input of the second OR gate, whose output is connected to the second inputs of the seventh flip-flop and the second pulse counting device, as well as to the input of the second pulse generator, whose output is connected to the second input of the third pulse counting device, the first input of which is connected to the output of the sixth AND gate. The output digital bus is connected to the first input digital buses of the digital comparator and the register; the first output digital bus of the register is connected to the second input digital bus of the digital comparator, whose output is connected to the first input of the register, and whose second output digital bus is connected to the input digital bus of the display unit. Two optical isolation units, a voltage filter, a current filter, a resistor temperature sensor, a resistor minimum temperature unit, a maximum resistor temperature value unit, the seventh and eighth comparators, the seventh and eighth NOT gates, the seventh and eighth flip-flops, the seventh and eighth AND gates, and the fourth XOR gate. The input of the first optical isolation unit is connected to the output of the current sensor. The output is connected to the input of the current filter. The output of the current filter is connected to the second input of the first comparator and the first input of the second comparator. The input of the second optical isolation unit is connected to the output of the voltage sensor, and its output is connected to the input of the voltage filter. The output of the voltage filter is connected to the second input of the third comparator and the first input of the fourth comparator. The output of the resistor temperature sensor is connected to the second input of the seventh comparator and to the first input of the eighth comparator, whose second input is connected to the output of the resistor temperature maximum value unit. The output of the minimum temperature value unit is connected to the first input of the seventh comparator, whose output is connected to the first input of the seventh NOT element, whose output is connected to the first input of the seventh flip-flop, whose output is connected to the first input of the seventh AND element. The output of the eighth comparator is connected to the first input of the eighth NOT gate, whose output is connected to the first input of the eighth flip-flop, whose output is connected to the second input of the seventh AND gate. The output of the seventh AND gate is connected to the first input of the fourth XOR gate. The output of the first OR element is connected to the second inputs of the seventh and eighth flip-flops, as well as the seventh and eighth NOT elements. The fourth output of the sample logic-time function unit is connected to the second input of the fourth XOR gate, whose output is connected to the fourth input of the switch. The first and fourth outputs of the second pulse counting device are connected to the first and second inputs of the eighth AND element, respectively, and its output is connected to the input of the digital comparator and to the second input of the second OR element.