Asynchronous RS flip-flop with a single feedback loop consists of NOT, AND, and OR logic gates. An asynchronous RS flip-flop is asymmetric and has a single feedback loop, where the first input (S input) is connected to the first input of the OR gate, the second input (R input) is connected via a NOT gate to the first input of the AND gate, whose output is connected to the second input of the OR gate, whose output serves as the flip-flop's output and is connected to the second input of the AND gate.