Device for thermal imaging diagnostics of hydrogenerator rotor windings comprises an infrared receiver with n individual infrared sensors, a frequency divider, a buffer register, a commutator, a data preparation unit, two pulse generators, two controlled amplifiers, a video control unit, two counters, a voltage generator, a memory unit, a position sensor, a position setting unit, a speed setting unit, a clock distributor, five registers, three digital comparators, a digital adder, two flip-flops, three AND elements, an analog-to-digital converter, a signal shaper, a first comparator, and two digital indicators. An output of the frequency divider is connected to inputs of the buffer register, the first counter, and to a first input of the video control unit, the second and third inputs of which are connected to outputs of the first and second controlled amplifiers, the first inputs of which are connected to an output of the voltage generator. Second inputs are connected, respectively, to first and second outputs of the memory unit, an input digital bus of which is connected to an output digital bus of the first counter. A first input of the data preparation unit together with a fourth input of the video control unit are connected to an output of the commutator, an input digital bus of which is connected to an output digital bus of the buffer register, an input digital bus of which is connected to outputs of n individual infrared sensors of the infrared receiver. An output of the data preparation unit is connected to computer circuits, an output digital bus of the position setting unit is connected to a first input digital bus of the first digital comparator, a second input digital bus of which together with input digital buses of the first and second registers are connected to an output digital bus of the position sensor. An output of the first digital comparator is connected to a first input of the first AND element, a second input of which is connected to a first output of the second flip-flop. An output is connected to a first input of the first flip-flop, a second input of which is connected to a second output of the second flip-flop, a first input of which is connected to an output of the second digital comparator, a second input digital bus of which is connected to an output digital bus of the speed setting unit. A first input digital bus is connected to an output digital bus of the digital adder. First and second input digital buses of the digital adder are connected, respectively, to output digital buses of the first and second registers, inputs of which are connected, respectively, to first and second outputs of the clock distributor, a third output of which is connected to a second input of the second flip-flop. An output of the second pulse generator is connected to an input of the clock distributor. An output of the first flip-flop is connected to a first input of the second AND element, a second input of which is connected to an output of the first pulse generator. An output is connected to inputs of the frequency divider, the voltage generator, the commutator, and to a second input of the data preparation unit. An output digital bus of the analog-to-digital converter is connected to an input digital bus of the third register, an output digital bus of which is connected to an input digital bus of the fourth register and to a first input digital bus of the third digital comparator, a second input digital bus of which is connected to the output digital bus of the analog-to-digital converter. An output is connected to a second input of the third AND element, a first input of which together with a second input of the analog-to-digital converter are connected to the output of the second AND element, and an output is connected to the input of the third register. The output of the commutator is connected to a first input of the analog-to-digital converter and to an input of the first comparator, an output of which is connected to a first input of the second counter, an output digital bus of which is connected to an input digital bus of the fifth register. A second input is connected to an output of the signal shaper, an input of which together with inputs of the fourth and fifth registers are connected to the output of the first digital comparator. Output digital buses of the fourth and fifth registers are connected respectively to input digital buses of the first and second digital indicators. There are introduced therein three counters, three registers, three AND elements, an OR element, a third flip-flop, a second comparator, a fourth digital comparator, a pulse shaper, and a third digital indicator. The output of the frequency divider is connected to an input of the third flip-flop, first and second outputs of which are connected, respectively, to first inputs of the fourth and fifth AND elements, outputs of which are connected to first inputs of the sixth and seventh registers, and second inputs together with a second input of the sixth AND element are connected to an output of the second comparator, an input of which is

connected to the output of the commutator. A first input of the sixth AND element is connected to an output of the fourth digital comparator, first and second input digital buses of which are connected, respectively, to output digital buses of the sixth and seventh registers, input digital buses of which are connected to an output digital bus of the third counter, and second inputs of which together with an input of the pulse shaper and an input of the eighth register are connected to an output of the OR element, a first input of which is connected to an output of the fourth counter, a first input of which is connected to the output of the third counter. A second input together with second inputs of the third counter and the OR element are connected to the output of the first digital comparator. The output of the pulse shaper is connected to a second input of the fifth counter, a first input of which is connected to the output of the sixth AND element. An output digital bus is connected to an input digital bus of the eighth register, an output digital bus of which is connected to an input digital bus of the third digital indicator. A first input of the third counter is connected to the output of the second AND element.