Device for thermal imaging diagnostics of hydrogenerator rotor windings comprises n individual infrared sensors, a position setting unit, three digital comparators, four AND gates, four triggers, two pulse generators, a frequency divider, a buffer register, a position sensor, three registers, a clock distributor, an adder, a speed setting unit, a commutator, a controlled frequency divider, a data preparation unit, a memory unit, a first counter, a video control unit, two controlled amplifiers, and a voltage generator. Wherein n outputs of an infrared receiver are connected to an input bus of the buffer register. The position setting unit and the position sensor are connected by their output digital buses, respectively, to first and second input digital buses of a first digital comparator, an output of which is connected to a first input of a first AND gate, an output of which is connected to a first input of a first trigger, an output of which is connected to a first input of a second AND gate, an output of which is connected to a first input of the data preparation unit and to inputs of the frequency divider, the commutator, and the voltage generator, an output of which is connected to second inputs of the first and second controlled amplifiers, outputs of which are connected, respectively, to third and second inputs of the video control unit. An output of the frequency divider is connected to a first input of the video control unit and to an input of the buffer register, an output digital bus of which is connected to an input digital bus of the commutator, an output of which is connected to a second input of the data preparation unit and to a fourth input of the video control unit. An output digital bus of the first counter is connected to an input digital bus of the memory unit, first and second outputs of which are connected to first inputs, respectively, of the second and first controlled amplifiers. An output digital bus of the position sensor is connected to input digital buses of first and second registers, output digital buses of which are connected to first and second input digital buses of a digital adder. An output of the data preparation unit is connected to computer circuits. An output digital bus of the speed setting unit is connected to a second input digital bus of a second digital comparator. An output digital bus of the digital adder is connected to an input digital bus of a third register, an output digital bus of which is connected to a first input digital bus of the second digital comparator and to an input digital bus of the controlled frequency divider, an input of which is connected to an output of the second pulse generator. An output of the controlled frequency divider is connected to a second input of the second AND gate. First and second outputs of the clock distributor are connected to inputs of the first and second registers, respectively, and a third output is connected to an input of the third register. Output digital buses of the first and second registers are connected to first and second input digital buses of a third digital comparator, respectively, first and second outputs of which are connected, respectively, to first inputs of second and third triggers, outputs of which are connected, respectively, to first inputs of third and fourth AND gates, outputs of which are connected to first and second inputs of the first counter, respectively. An output of the second digital comparator is connected to a first input of a fourth trigger, an output of which is connected to a second input of the first AND gate. Second inputs of the second, third, and fourth triggers are connected to the third output of the clock distributor. Second inputs of the third and fourth AND gates are connected to the output of the frequency divider. An output of the first pulse generator is connected to an input of the clock distributor. Furthermore, three counters, three registers, three AND gates, an OR gate, a NOT gate, a fifth trigger, a comparator, a fourth digital comparator, a pulse shaper, and a digital indicator are introduced into the device. Wherein the output of the frequency divider is connected to an input of the fifth trigger, first and second outputs of which are connected, respectively, to first inputs of fifth and sixth AND gates, outputs of which are connected to first inputs of fourth and fifth registers, and second inputs of which, together with a second input of a seventh AND gate, are connected to an output of the comparator, an input of which is connected to the output of the commutator. A first input of the seventh AND gate is connected to an output of the fourth digital comparator, first and second input digital buses of which are connected, respectively, to output digital buses of the fourth and fifth registers, input digital buses of which are connected to an output digital bus of a second counter, and second inputs of which, together with an input of the pulse shaper and an input of a sixth register, are connected to an output of the OR gate, a first input of which is connected to an

output of a third counter, a first input of which is connected to the output of the second counter, and a second input of which, together with second inputs of the second counter and the OR gate, is connected to the output of the first digital comparator. An output of the pulse shaper is connected to a second input of a fourth counter, a first input of which is connected to the output of the seventh AND gate. An output digital bus is connected to an input digital bus of the sixth register, an output digital bus of which is connected to an input digital bus of the digital indicator. A first input of the second counter is connected to the output of the second AND gate, an output of the fourth trigger is connected to an input of the NOT gate, an output of which is connected to the second input of the first trigger.